What is claimed is:

1. An electrostatic discharge (ESD) protection circuit in a semiconductor integrated circuit (IC) having protected circuitry, the ESD protection circuit comprising:

an SCR for shunting ESD current away from said protected circuitry, said SCR comprising:

a substrate;

an N-well and an adjacent P-well formed over said substrate and defining a PN junction therebetween;

an insulator layer formed over said substrate and electrically isolating said N-well and P-well from said substrate;

an N+ cathode region formed in said P-well and for coupling to ground;

a P+ anode region formed in said N-well and for coupling to a pad of said protected circuitry;

at least one P+ trigger tap region disposed in said P-well and spaced proximate to said N+ cathode region, said at least one P+ trigger tap being adapted to trigger said SCR; and

at least one N+ trigger tap region disposed in said N-well and spaced proximate to said P+ anode region, said at least one N+ trigger tap being adapted to trigger said SCR.

2. The ESD protection circuit of claim 1, wherein said at least one P+ trigger tap region comprises two P+ trigger tap regions, where each P+ trigger tap region is disposed axially in-line and at opposing ends of said N+ cathode region in said P-well.

3. The ESD protection circuit of claim 1, wherein said at least one N+ trigger tap region comprises two N+ trigger tap regions, where each N+ trigger tap

region is disposed axially in-line and at opposing ends of said P+ anode region in said N-well.

4. The ESD protection circuit of claim 1, wherein said insulator layer is selected from the group of materials comprising SiO_2 and sapphire.

5. The ESD protection circuit of claim 1, wherein a surface area over a non-high-doped region and between the N+ cathode region and the P+ anode region is shallow trench isolation (STI) blocked.

6. The ESD protection circuit of claim 1, wherein a surface area of the N-well and P-well between the N+ cathode region and the P+ anode region is silicide blocked.

7. The ESD protection circuit of claim 1, wherein said SCR is self-triggering, in an instance where said at least one P+ trigger tap and N+ trigger tap are respectively coupled to said N+ cathode and P+ anode, and wherein a voltage applied across said N+ trigger tap region and said P+ trigger tap has a potential exceeding a threshold to create a depletion region formed entirely between said N+ cathode region formed in said P-well and said P+ anode region formed in said N-well.

8. The ESD protection circuit of claim 7, wherein said depletion region comprises:

a first depletion layer formed at a P+N junction proximately between the P+ anode region and the N-well in an instance where said P+ anode and said N-well are at a same potential;

a second depletion layer formed at a PN+ junction proximately between the N+ cathode region and the P-well, in an instance where said P-well and N+ cathode region are at a same potential; and

a third depletion layer formed proximately between the said P-well and N-well, in an instance where said PN junction is reversed biased.

9. The ESD protection circuit of claim 8, wherein in an instance where said third depletion layer reaches said first and second depletion layers, said N-well and P-well between said P+ anode and N+ cathode regions are entirely depleted of carriers and become intrinsically conducting to form said depletion region.

10. The ESD protection circuit of claim 1, wherein an N-channel is formed in said N-well between said P+ anode region and said insulator layer, and a P-channel is formed in said P-well between said N+ cathode region and said insulator layer.

11. The ESD protection circuit of claim 10, wherein said N-channel and P-channel respectively have higher doping concentrations than the N-well and P-well.

12. The ESD protection circuit of claim 11, wherein a first STI region and a second STI region are respectively formed over a portion of said N-channel and said P-channel.

13. The ESD protection circuit of claim 12, wherein said first STI region is formed between said at least one N+ trigger tap region and said P+ anode region, and said second STI region is formed between said at least one P+ trigger tap region and said N+ cathode region.

14. The ESD protection circuit of claim 13, wherein said at least one P+ trigger tap region extends a length parallel to said N+ cathode region in said P-well.

15. The ESD protection circuit of claim 14, wherein said at least one N+ trigger tap region extends a length parallel to said P+ anode region in said N-well.

16. The ESD protection circuit of claim 1, further comprising:

a triggering device having at least a first and second terminal coupled to the SCR, wherein said first terminal is for coupling to the pad and said second terminal is coupled to said at least one P+ trigger tap region.

17. The ESD protection circuit of claim 16, wherein the triggering device comprises a NMOS transistor wherein a source and a drain of the NMOS transistor are respectively coupled to said P+ trigger-tap region and for coupling to the pad.

18. The ESD protection circuit of claim 17, wherein a gate of the NMOS is coupled to the source of the NMOS transistor.

19. The ESD protection circuit of claim 16, wherein the triggering device comprises at least one diode serially coupled in a forward conduction direction between said pad and said at least one P+ trigger tap.

20. The ESD protection circuit of claim 1, further comprising:

a triggering device having at least a first and second terminal coupled to the SCR, wherein said first terminal is for coupling to ground and said second terminal is coupled to said at least one N+ trigger tap region.

21. The ESD protection circuit of claim 20, wherein the triggering device comprises a PMOS transistor wherein a source and a drain of the PMOS transistor are respectively coupled to said N+ trigger-tap region and for coupling to ground.

22. The ESD protection circuit of claim 21, wherein a gate of the PMOS is coupled to the source of the PMOS transistor.

23. The ESD protection circuit of claim 20, wherein the triggering device comprises at least one diode serially coupled in a forward conduction direction between ground and said at least one N+ trigger tap.

24. The ESD protection circuit of claim 1, further comprising at least one PN junction diode serially coupled in a forward conduction direction between said pad and said P+ anode region.

25. An electrostatic discharge (ESD) protection circuit in a semiconductor integrated circuit (IC) having protected circuitry, the ESD protection circuit comprising:

an SCR for shunting ESD current away from said protected circuitry, said SCR comprising:

a substrate;

an N-well and an adjacent P-well formed over said substrate and defining a PN junction therebetween;

an insulator layer formed over said substrate and electrically isolating said N-well and P-well from said substrate;

an N+ cathode region formed in said P-well and coupled to ground;

a P+ anode region formed in said N-well and coupled to a pad of said protected circuitry;

an integrated trigger device, comprising:

an N+ drain region, formed in said P-well and coupled to said pad, and defining an NMOS channel therebetween said N+ cathode region;

a gate region, coupled to said N+ cathode region, and disposed over said NMOS channel;

at least one P+ trigger tap region disposed in said P-well and spaced proximate to said N+ cathode region and said N+ drain region, said at least one P+ trigger tap being adapted to trigger said SCR; and

at least one N+ trigger tap region disposed in said N-well and spaced proximate to said P+ anode region, said at least one N+ trigger tap being adapted to trigger said SCR.

26. The ESD protection circuit of claim 25, wherein said at least one P+ trigger tap region comprises two P+ trigger tap regions, where each P+ trigger tap region is disposed axially in-line and at opposing ends of said N+ cathode region and said N+ drain region in said P-well.

27. The ESD protection circuit of claim 26, wherein said at least one N+ trigger tap region comprises two N+ trigger tap regions, where each N+ trigger tap region is disposed axially in-line and at opposing ends of said P+ anode region in said N-well.

28. The ESD protection circuit of claim 25, wherein said insulator layer is selected from the group of materials consisting of SiO_2 and sapphire.

29. The ESD protection circuit of claim 25, wherein a surface area over a non-high-doped region and between the N+ cathode region and the P+ anode region is shallow trench isolation (STI) blocked.

30. The ESD protection circuit of claim 25, wherein a surface area of the N-well and P-well between the N+ cathode region and the P+ anode region is silicide blocked.

31. The ESD protection circuit of claim 25, further comprising at least one PN junction diode serially coupled in a forward conduction direction between said pad and said P+ anode region.